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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,221	04/13/2004	Se-Hoon Oh	5649-1228	4644

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EXAMINER	
GURLEY, LYNNE ANN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,221	OH ET AL.	
	Examiner	Art Unit	
	Lynne A. Gurley	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment and remarks filed 10/14/05.

2. Currently, claims 9-27 are pending.

Response to Arguments

3. Applicant's arguments, see page 8, filed 10/14/05, with respect to the rejection(s) of claim(s) 9-27 under 35 USC 102 and 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Applicant's Admitted Prior Art in view of Derraa et al. (US 6,696,368).

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

6. Claim 25 is objected to because of the following informalities: in line 2, "at a temperature **of about from about** 600 to about 900" is redundant . Changing to "at a temperature from about 600 to about 900" is suggested. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 22-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. In claim 22, line 7, the term "first etch stop" and, in claim 23, line 2, the term "second etch stop" are indefinite in that the first etch stop is defined in the specification as being on top of the buried contact plug *instead of* on top of the first pad contact plug, the second pad contact plug and the first interlayer dielectric layer as in the claim. The second etch stop is disclosed as being on top of the first interlayer dielectric. It is suggested that the position of the first etch stop be amended so that it does not conflict with the position of the second etch stop.

10. Claim 27 recites the limitation "the etch stop layer" in lines2 and 3. There is insufficient antecedent basis for this limitation in the claim. Specifically, a first and a second etch stop layer have been previously introduced in the claims. Clarification as to whether "the etch stop layer" is the first etch stop layer or the second etch stop layer is requested.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 9-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (specification, pages 1-2 and figure 1) in view of Derraa et al. (US 6,696,368, dated 2/24/04, filed 7/31/01).

Applicant's Admitted Prior Art shows the method as claimed in figure 1 and corresponding text of the specification, pages 1-2, with buried contact plug 5 on cell array region A; resistor 15 on peripheral circuit region B; first pad contact plug 11; second pad contact plug (in metal contact hole 24, page 2, lines 24-25); and ohmic layer 26 between the second pad contact plug (in metal contact hole 24, page 2, lines 24-25) and the resistor 15. The lower interlayer dielectric 3 is shown. The first interlayer dielectric 9 is shown. The capacitor 18/19/21 is formed. Etch stop layers 7 and 17 are shown. The second interlayer dielectric is shown.

Applicant's Admitted Prior Art lacks anticipation only in not teaching that: 1) an ohmic layer is formed between the first pad contact plug and the buried contact plug in the cell array region (or, on floor of the first pad contact holes) of an integrated circuit substrate; 2) the first interlayer dielectric layer formed on the lower interlayer dielectric layer, the buried contact plug and the resistor defines a second pad contact hole in the peripheral circuit region; 3) the first interlayer dielectric layer defines a second pad contact hole in the peripheral circuit region and wherein the second pad contact plug is disposed in the second pad contact hole; 4) a first adhesion layer is formed between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and a second adhesion layer is formed between the metal contact plug and the

second interlayer dielectric layer and between the metal contact plug and the second pad contact plug; 5) patterning the first conductive layer to provide a buried contact plug in the contact hole in the cell array region and a resistor on the lower interlayer dielectric layer in a peripheral circuit region of the integrated circuit substrate; 6) forming a second conductive layer on the ohmic layer and in the first pad contact hole; 7) the thermal treatment is performed at a temperature of about from 600 to about 900 degrees Celsius for from about 10 to about 30 seconds; and, 8) a mold layer is formed on the etch stop layer and the subsequent processing steps of forming the capacitor (claim 27).

Derraa teaches a conventional method of forming a reliable contact plug to a cell array region such as a buried contact region wherein the contact region is first covered with a silicide and then filled with a conductive layer or layers (column 3, lines 54-57; column 4, lines 25-30, lines 42-46, lines 49-60; column 5, lines 45-53). The contact improves adhesion of the conductive layer to the surrounding insulating layers and lowers the resistance of the contact by forming the silicide.

It would have been obvious to one of ordinary skill in the art to have had: 1) an ohmic layer formed between the first pad contact plug and the buried contact plug in the cell array region (or, on floor of the first pad contact holes) of an integrated circuit substrate; and 6) a second conductive layer formed on the ohmic layer and in the first pad contact hole, in the method of Applicant's Admitted Prior Art, with the motivation that Derraa teaches that a silicide layer (ohmic layer) is conventionally formed in a contact to a cell array region, with the purpose of reducing the resistance of the contact and of making the contact more reliable, therefore the

incorporation of such an ohmic layer in Applicant' Admitted Prior art structure would be conventional and an improvement of the contact configuration and reliability.

It would have been obvious to one of ordinary skill in the art to have had: 4) a first adhesion layer formed between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and a second adhesion layer is formed between the metal contact plug and the second interlayer dielectric layer and between the metal contact plug and the second pad contact plug; in the method of Applicant's Admitted Prior Art, with the motivation that Derraa teaches that adhesion layers are important to the reliability of the contact and is already included in the conductive layers in the plug, so that the inclusion of an adhesion layer would be conventional.

It would have been obvious to one of ordinary skill in the art to have had: 2) the first interlayer dielectric layer formed on the lower interlayer dielectric layer, the buried contact plug and the resistor defines a second pad contact hole in the peripheral circuit region; 3) the first interlayer dielectric layer define a second pad contact hole in the peripheral circuit region and wherein the second pad contact plug is disposed in the second pad contact hole; 5) the first conductive layer patterned to provide a buried contact plug in the contact hole in the cell array region and a resistor on the lower interlayer dielectric layer in a peripheral circuit region of the integrated circuit substrate, in the method of Applicant's Admitted Prior Art, with the motivation that the formation of the first conductive layer patterned to provide a buried contact plug in the contact hole in the cell array region and a resistor on the lower interlayer dielectric layer in a

peripheral circuit region of the integrated circuit substrate, would decrease the number of patterning steps involved in the process, thereby increasing efficiency.

It would have been obvious to one of ordinary skill in the art to have had: 7) the thermal treatment performed at a temperature of about from 600 to about 900 degrees Celsius for from about 10 to about 30 seconds, in the method of Applicant's Admitted Prior art, with the motivation that Derraa teaches that these temperatures and times intervals are conventional for forming a silicide in a contact.

Additionally, it would have been obvious to one of ordinary skill in the art to have had: 8) a mold layer formed on the etch stop layer and the subsequent processing steps of forming the capacitor (claim 27), in the method of Applicant's Admitted Prior Art, with the motivation that these steps are conventional to form the type of capacitor shown in figure 1 of Applicant's disclosure.

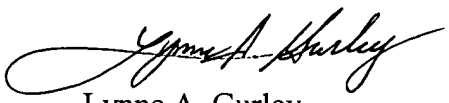
Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley
Primary Patent Examiner
TC 2800, Art Unit 2812

LAG
January 31, 2006